Laboratorium Module of Digital Electronics

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LABORATORIUM ELEKTRONIKA
DAN INSTRUMENTASI

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List of Content

LAB 1
LOGIC GATES

Learning Objective

1. Understanding the symbols of logic gates in digital circuits.
2. Ability to create logic gate circuits using simulation software.
3. Ability to create truth tables for logic gate circuits.

Supporting Theory

Logic gates are fundamental components of every digital electronic circuit. Among several known logic gates, there are some basic logic gates that can be further developed into other logic gates in their application. These basic gates are:

- OR Gate
- AND Gate
- NOT Gate (Inverter)
- XOR Gate

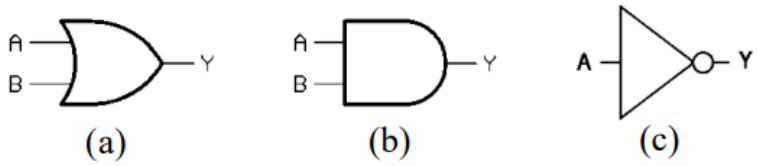


Figure.1. Symbol for (a) OR gate, (b) AND gate, and (c) NOT gate

From these logic gates, other logic gates can be created. For example, NOR gate is a combination of an OR gate and a NOT gate, while NAND gate is a combination of an AND gate and a NOT gate, and so on

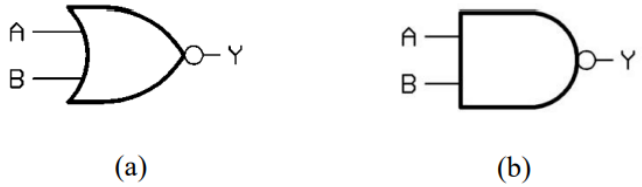


Figure.2. Symbol for (a) NOR gate, (b) NAND gate

In addition, there is also a type of logic gate called the Exclusive Logic Gate. Exclusive Logic Gates include only OR and NOR gates. The symbols are typically as shown below:

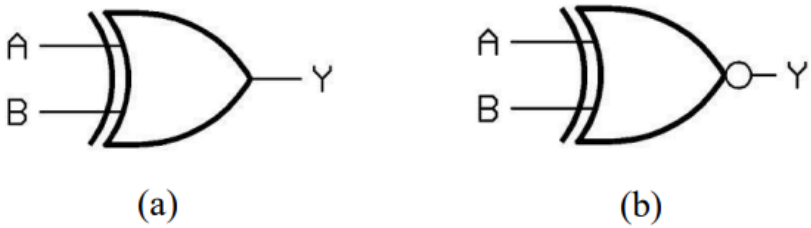
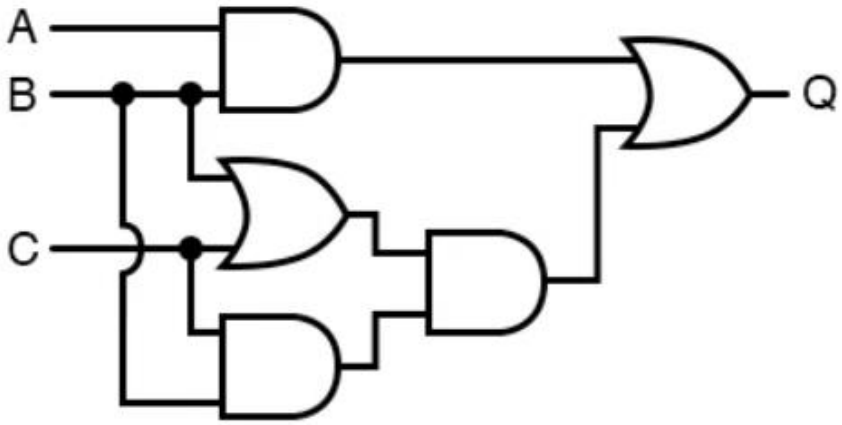


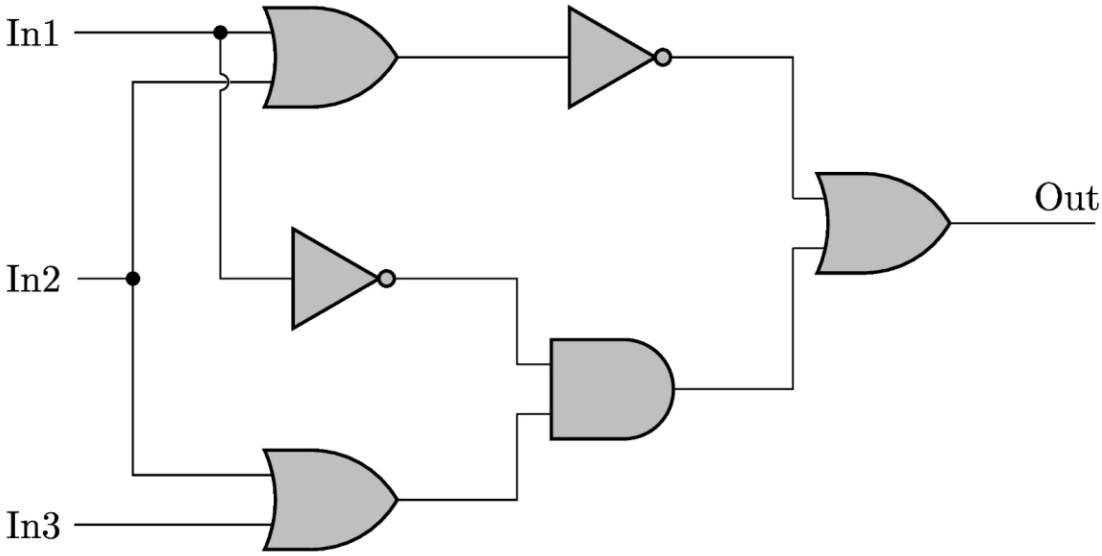
Figure.3. Symbol for (a) XOR gate, (b) XNOR gate

Digital Electronics Lab Assignment

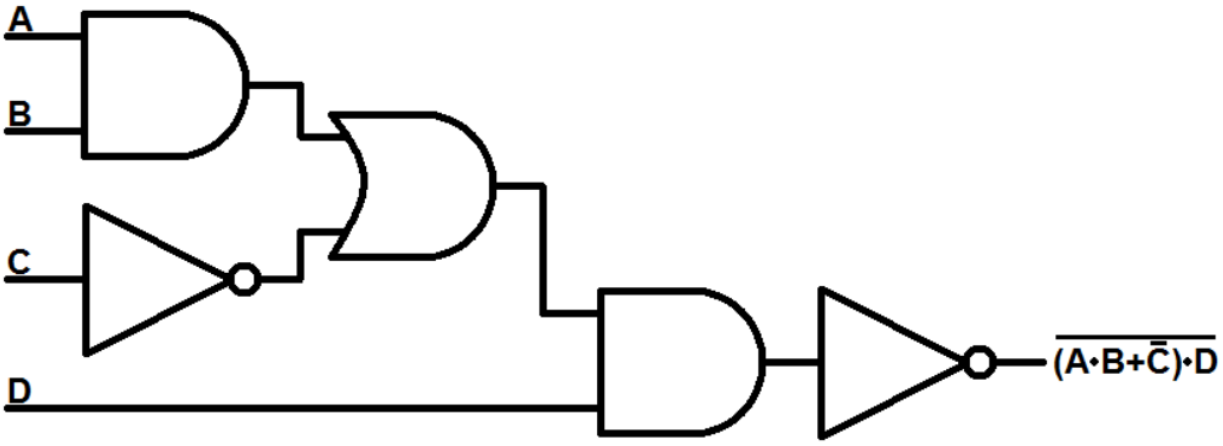
1. Create circuit simulations for logic gates AND, OR, NOT, NOR, NAND, XOR, and create their truth tables.
2. Create circuits as described below and write their truth tables.
    a. Circuits 1



b. Circuit 2



c. Circuit 3



LAB 2
ADDER

Learning Objective

1. Understanding half adder and full adder circuits.
2. Proficiency in assembling adder circuits.
3. Understanding binary number addition in digital circuits.

Supporting Theory

1. Half Adder

A half adder is a combinational logic circuit designed by combining XOR and AND gates. The half adder circuit has two inputs: A and B, each of which produces an output for carry and sum.

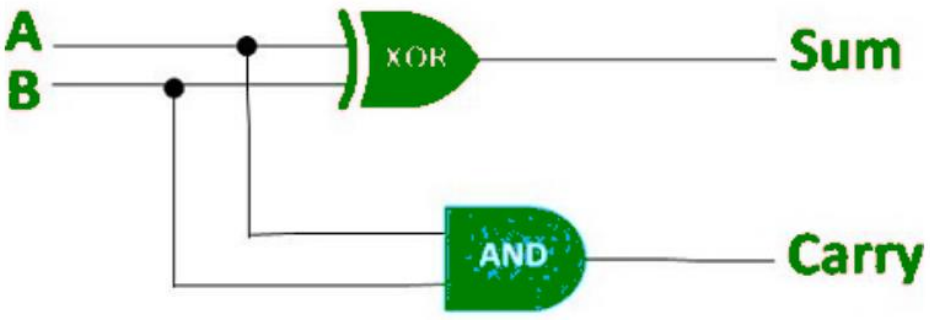


Figure.1. Half adder circuits

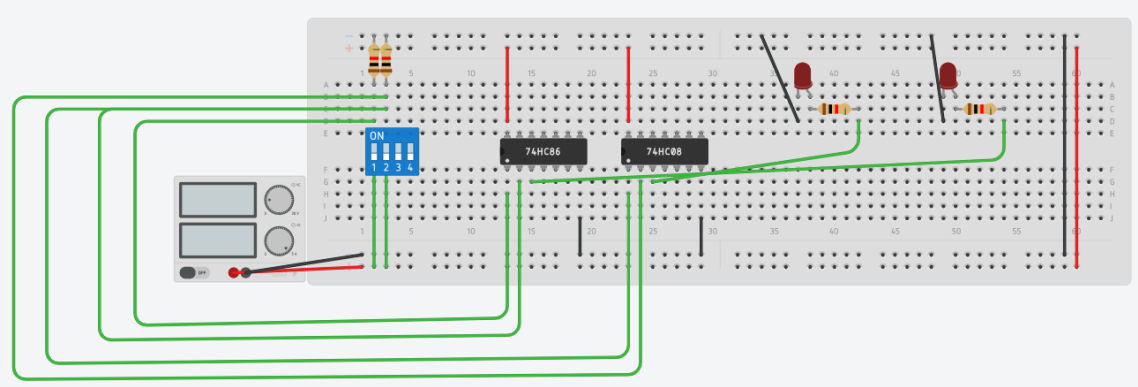


Figure.2. Half Adder circuit arrangement

Experiment Instruction:

Create a truth table for the half-adder circuit.

A	B	Sum	Carry
0	0		
0	1		
1	0		
1	1		

2. Full Adder

A full adder is a circuit composed of two XOR gates, two AND gates, and one OR gate. A full adder is an adder that sums three inputs and produces two outputs. The first two inputs are represented as A and B, while the third input is called C-IN (carry-in). In essence, a full adder is a combination of two half-adder circuits.

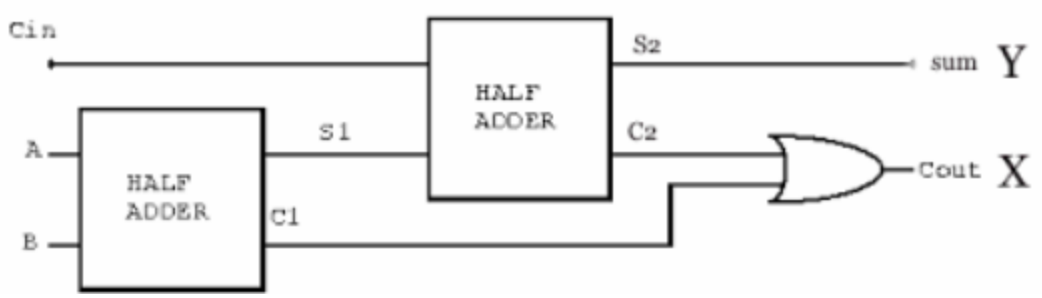


Figure.3. Full adder circuit which consist of 2 half adder circuits

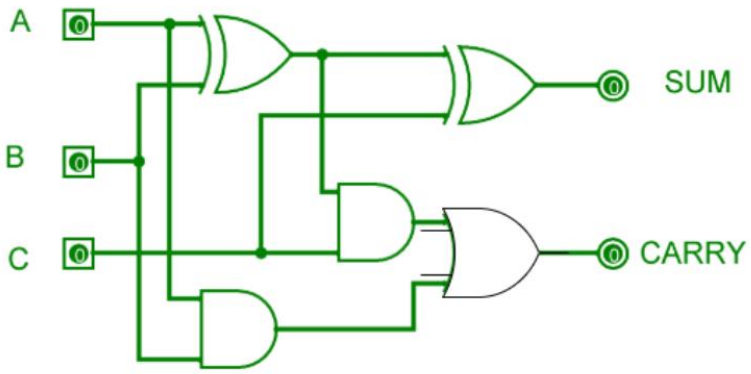


Figure.4. Full adder gate circuit

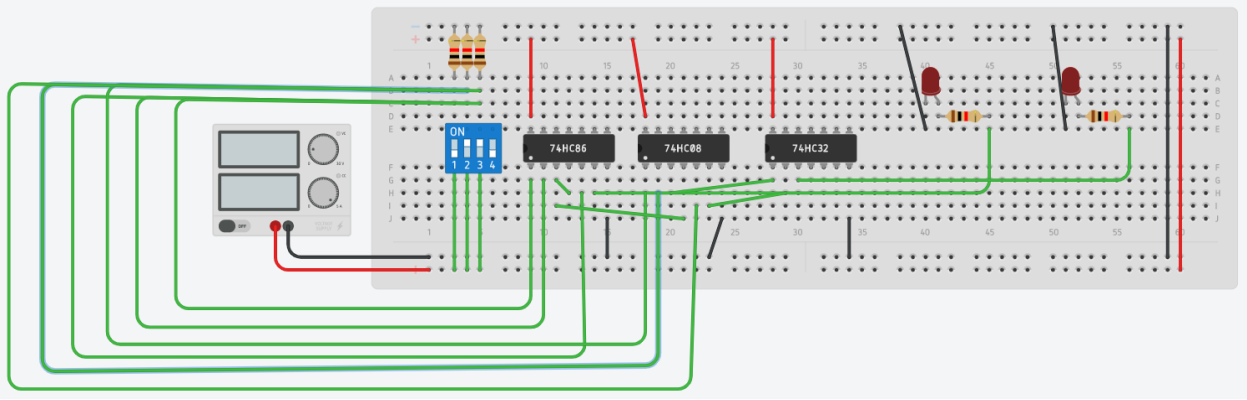


Figure.5. Full adder circuit using IC component

Experiment Instruction:

Create a truth table for the half-adder circuit.

A	B	C	Sum	Carry

0	1	0		
1	0	0		
0	0	1		
1	0	1		
0	1	1		
1	1	1		

3. Full Adder

By using a full adder circuit, mathematical addition operations on binary numbers can be performed in digital circuits. With the ability of an adder to perform mathematical operations, adders are typically found in the Arithmetic Logic Unit (ALU) of a computer system.

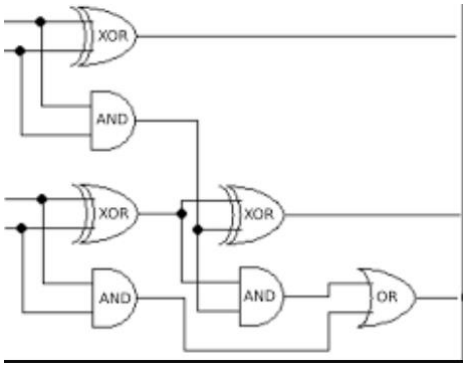


Figure.6. Block diagram of adder 2 bit

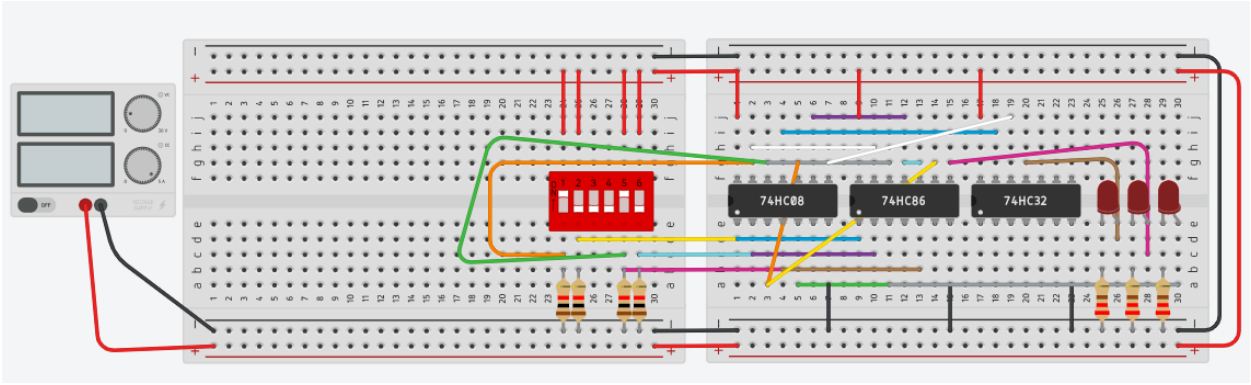


Figure.7. Circuit scheme of adder 2 bit

Experiment Instruction:

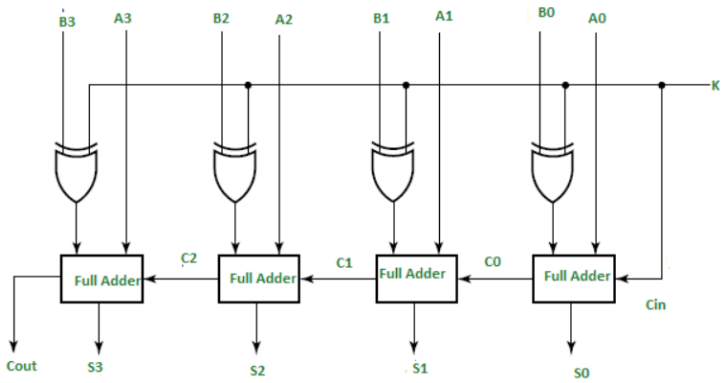
Create a truth table for the half-adder circuit.

A1	A2	B1	B2	Y1	Y2	Y3

0	1	0	0			
0	0	0	1			
0	1	0	1			
0	1	1	1			
1	1	0	1			
1	1	1	1			

4. 4-Bit Adder

A 4-bit adder is a circuit designed for addition operations in digital electronics with 4-bit data. In this section, similar to a 2-bit adder, it has a larger number of bits for addition. The circuit is constructed using a combination of full adders, as shown in the diagram.



Fiugre.8. Circuit of full adder

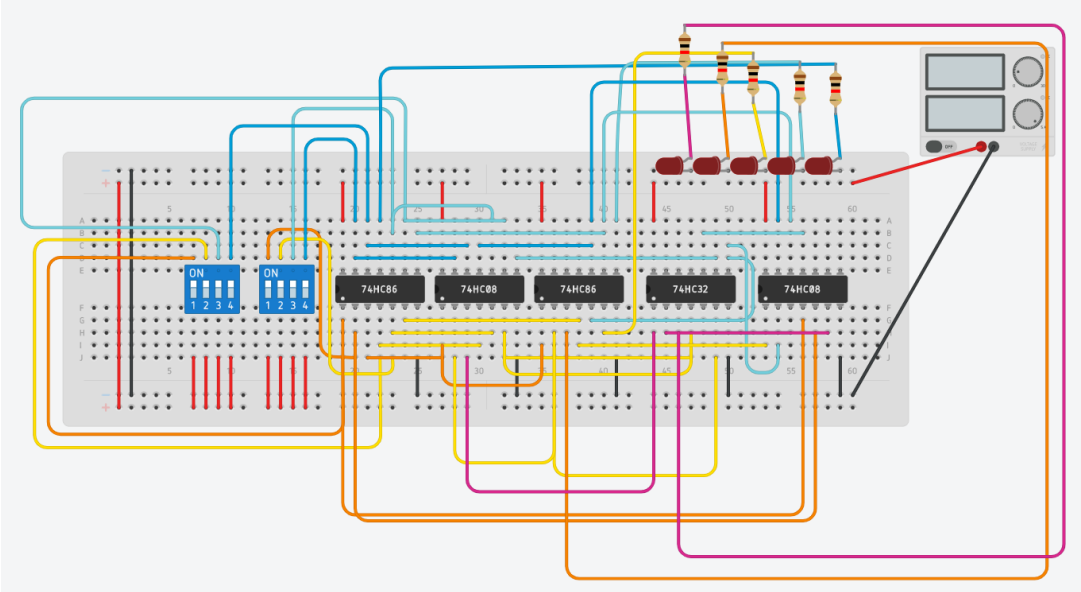


Figure.9. Circuits scheme of 4 bits adder

Experiment Instruction:

Create a truth table for the half-adder circuit.

A1	A2	A3	A4	B1	B2	B3	B4	Y1	Y2	Y3	Y4	Y5
0	0	0	1	0	0	0	1					
0	0	0	1	0	0	1	0					
0	0	0	1	0	1	0	0					
0	0	0	1	1	0	0	0					
0	0	0	1	0	0	1	1					
0	0	0	1	0	0	1	0					
etc												

LAB 3
MULTIPLEXER

Learning Objective

1. Understanding the Purpose of a Multiplexer
2. Able to Create Basic Multiplexer Circuit
3. Able to Select the Appropriate Data Output for a Given Input

Supporting Theory

A Multiplexer is a combinational logic circuit specifically designed to route one of several INPUT paths to a single OUTPUT path. The selected input path determines which input connects to the output. Multiplexers, often abbreviated as MUX or MPX, are essentially digital circuits made from high-speed logic gates used

to switch digital or binary data. They can also be of analog types that use components like transistors, MOSFETs, or relays to switch one input to an output. Multiplexers are also commonly referred to as Data Selector Devices.

Although they are solid-state devices made of semiconductors, Multiplexers operate like a rotary switch that is connected in series with a single-pole, single-throw (SPST) switch, as shown in the diagram below.

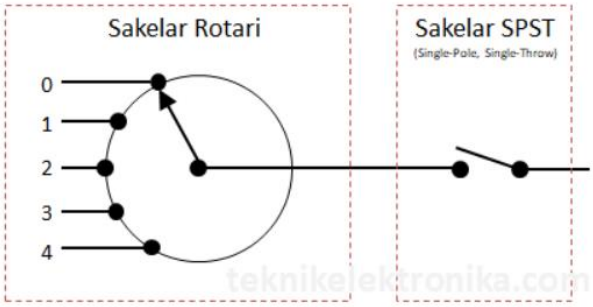


Figure.1. Mechanic multiplexer using relay

In Figure 1, the current entering the SPST switch will be connected to the value of the input current entering the rotary switch. Therefore, by using a relay, we can choose which input to use as the output.

The function of data selection, as shown in Figure 1, can be implemented using digital circuits by arranging appropriate logic gates. This allows us to choose a specific input data that will appear as the output. In a logic circuit, a multiplexer functions as a kind of data selector, selecting one of 2^N inputs based on the given code and passing it to the output.

2-Input Multiplexer

A 2-input multiplexer works by selecting one of the two inputs to be presented as the output of the multiplexer. The circuit for this is shown in Figure 2.

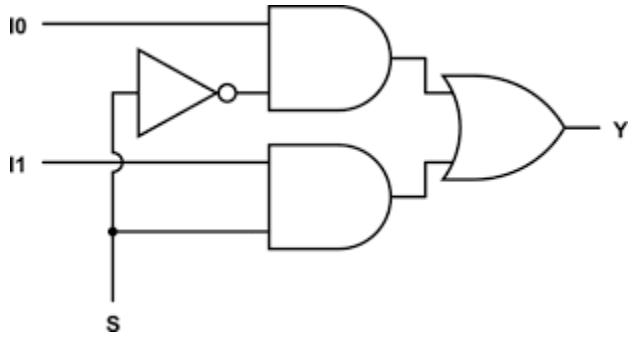


Figure.2. 2-input multiplexer circuit

Experimental Instruction

1. Create 2 – input multiplexer circuit
2. Fill the truth table

S	I_0	I_1	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

4 – Input Multiplexer

A 4-input multiplexer works by selecting one of the four inputs to be presented as the output of the multiplexer. The circuit for this is shown in Figure 3.

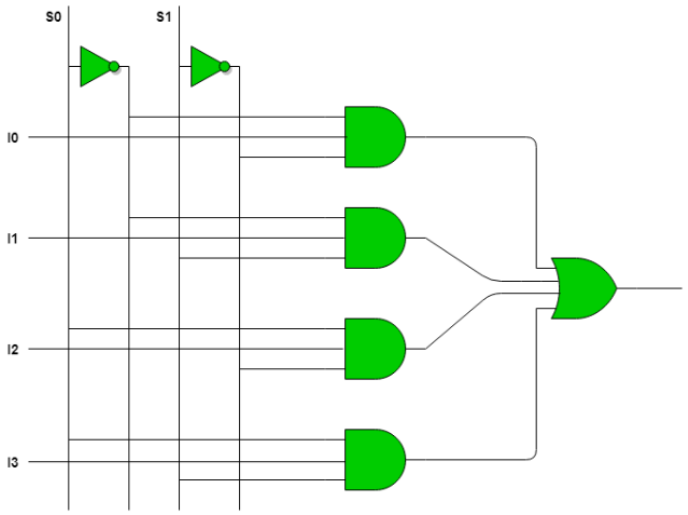


Figure.3. 4-Input multiplexer circuit

Experimental Instruction

1. Create 4-input multiplexer circuit
2. Fill the truth table

S_0	S_1	I_0	I_1	I_3	I_4	Y
0	0	0	0	0	0	
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
0	0	0	1	0	1	
0	0	0	1	1	0	
0	0	0	1	1	1	
0	0	1	0	0	0	
0	0	1	0	0	1	
0	0	1	0	1	0	
0	0	1	0	1	1	
0	0	1	1	0	0	
0	0	1	1	0	1	
0	0	1	1	1	0	
0	0	1	1	1	1	

LAB 4
LATCH CIRCUIT

Learning Objectives

- Understand the operation of a latch circuit.
- Able creating latch circuit

Supporting Theory

In the previous material, we have learned the combination of various logic gates to create a circuit with a specific output, which we refer to as a combinational circuit. A combinational circuit is a circuit whose output depends on the current input values. If the current input is changed, the output value will also change. In addition to combinational circuits, there are also sequential circuits, which are circuits whose inputs depend on the current input values and the previous output values. The block diagram of a sequential circuit is shown in Figure 1.

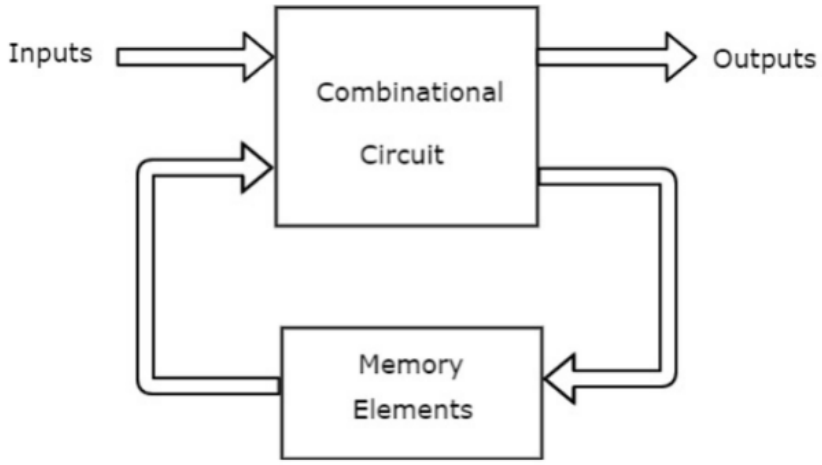


Figure.1. Sequential Circuit Scheme

Based on Figure 1, it can be observed that the output from the combinational circuit is reused as input for the subsequent results, or the previous result serves as input for the current state. Therefore, sequential circuits consist of both combinational circuits and memory storage elements. Some sequential circuits may not have a combinational circuit or may only consist of memory storage elements.

Memory Element Circuits

There are two types of memory elements based on the triggering mechanism to operate them, namely Latches and Flip-Flops. In a Latch, the triggering condition for the circuit to work is that the input value at the Emitters must be 1, while in a flip-flop circuit, the triggering condition is the change in input from 0 to 1 or an edge-sensitive signal boundary.

SR Latch

This circuit is also known as a Set-Reset Latch, which has three inputs: Reset, Set, and Enable. This circuit has two outputs, and the output results are influenced by the inputs when the Enable part is set to a value of 1. The circuit is shown in Figure 2.

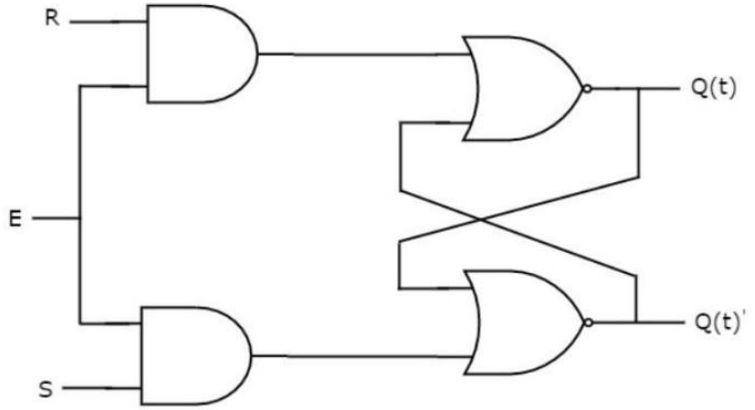


Figure.2. SR-Lacth Circuit Scheme

The output table obtained from the combination of S and R in the circuit above is shown as follows:

Table.1. Output of SR-Latch

S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

The table above is obtained by giving a value of 1 to input E. If input E is set to 0, then the output will not be affected by changes in the input. From the truth table results, it can be seen that when S is set to 1, the output Q will be set to 1. Meanwhile, when the R or Reset pin is set to 1, the output Q will be set to 0. When both S and R are set to 0, the output will retain its previous value, which is referred to as latch or memory.

Experimental Instruction

Create SR-Latch Circuit, and prove the truth table?

D Latch

The drawback of the SR Latch is that the next output cannot be predicted when both S and R values are set to 1. This is an invalid output state in the SR Latch. To address this difficulty, the D Latch is used. The circuit for the D Latch is shown in Figure 3.

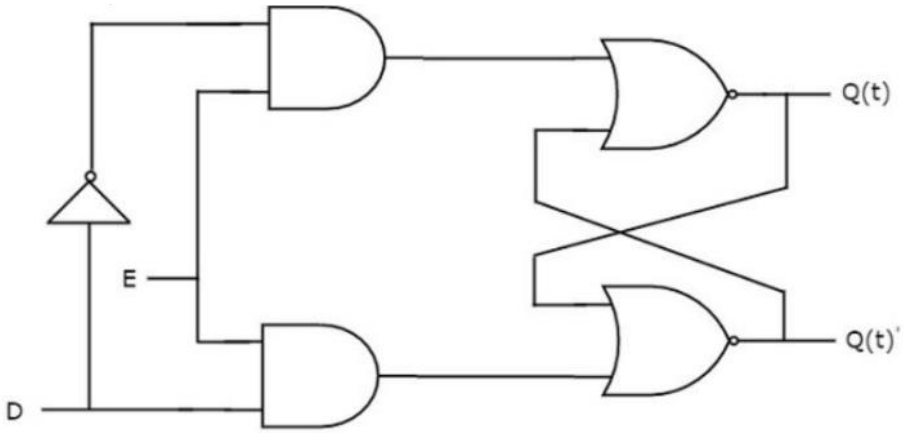


Figure.3. D-Latch circuit scheme

The state table for the D Latch circuit is shown as follows:

Table.2. The state table of D Lacth

E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

Experimental Instruction

Create D Latch circuit and prove the truth table of circuit

LAB 5
FLIP – FLOP

Learning Objectives

1. To understand and study the characteristics of Flip-Flop circuits.
2. To analyze the operation of Flip-Flops.
3. To be able to utilize Flip-Flops.

Supporting Theory

Flip-Flop is a circuit made up of digital components that has two opposing output states. Meanwhile, the input can vary. The basic idea of a Flip-Flop is a circuit made up of several NAND gates connected in such a way that it meets the criteria of a Flip-Flop as mentioned above.

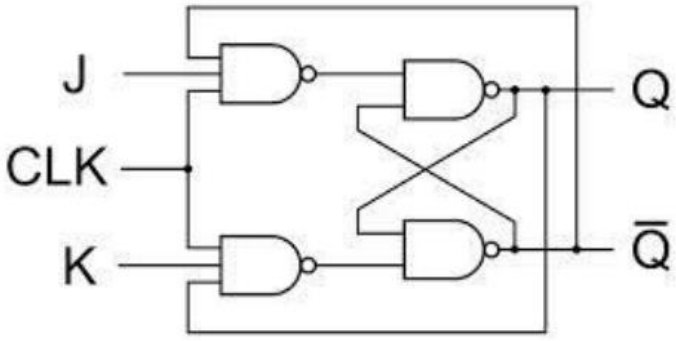
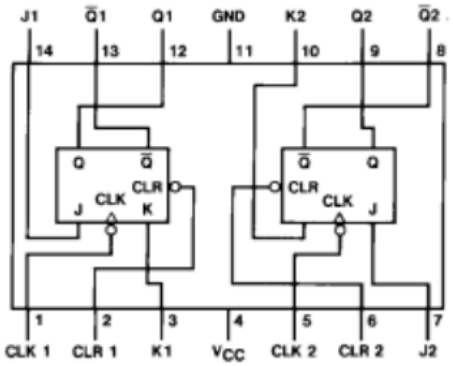


Figure.1. Circuit of JK Flip – Flop

IC 74LS73 Circuit Connection



Experimental Instruction

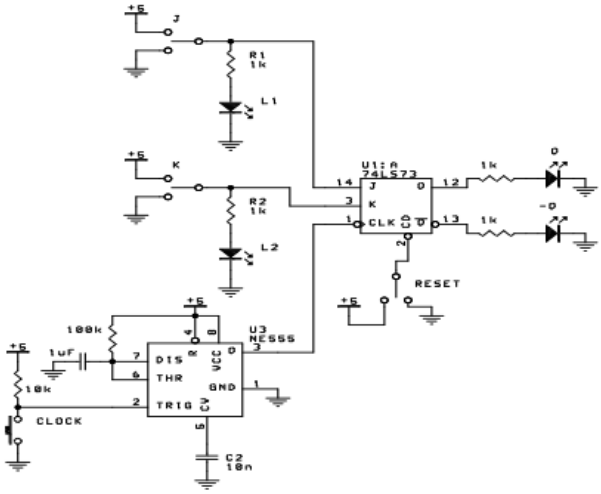


Figure.3. JK Flip – Flop Circuit

Observing Figure.3 above! The JK Flip-Flop uses the IC 74LS73. The inputs consist of J, K, and CLOCK, as well as outputs Q and -Q. All indicators for input and output use LEDs. For the CLOCK input, a monostable multivibrator is used to ensure a definite state at the rising edge. If the LED is on, it indicates logic '1', and if it is off, it indicates logic '0'.

The steps to perform this experiment are as follows:

1. Connect the power supply by plugging the connector into the board and turn on the power supply!
2. Then fill in table 1!
3. CLK ON: The CLOCK button is pressed and then released.
4. What conclusion can you draw?

Table 1 Data Results of JK Flip-Flop Circuit Experiment

RST	J	K	CLK	Q	-Q
0	X	X	X		
1	0	0	ON		
1	0	1	ON		
1	1	0	ON		
1	1	1	ON		

LAB 6
REGISTER

Learning Objectives

1. To study and investigate the properties of Shift Registers.
2. To understand the functions of Serial and Parallel Registers.
3. To be able to operate and assemble Registers.

Supporting Theory

A register is one form of a logic circuit, which is a combination of multiple Flip-Flops. There are several types of registers distinguished by their Input and Output types, including:

a) Serial Input Parallel Output (SIPO)

b) Parallel Input Parallel Output (PIPO)

This system can be constructed from all types of Flip-Flops practiced previously. Reading the output of the register is based on the shift of the pressed switch, while the logic of the shift is based on the initial input. Here, it's important to understand the terms MSB (Most Significant Bit) and LSB (Least Significant Bit).

a. Serial Input Parallel Output (SIPO)

IC 74LS157 and IC74LS164 Logic Connection

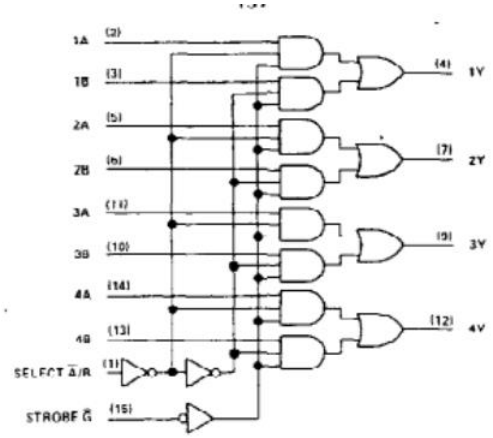


Figure.1. IC 74LS157

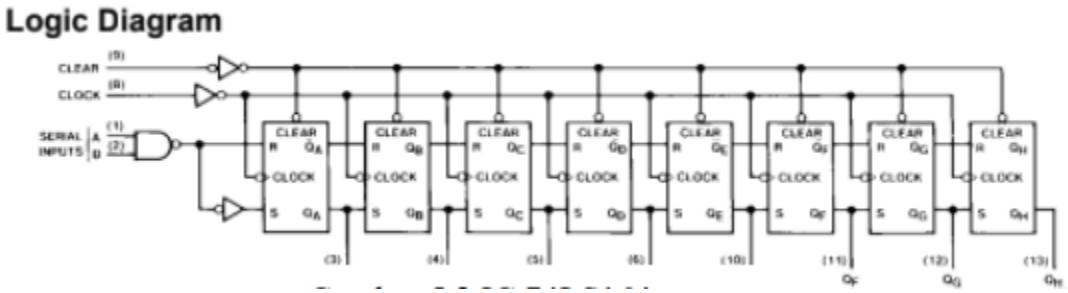


Figure.2. IC 74LS164

Experimental Instruction

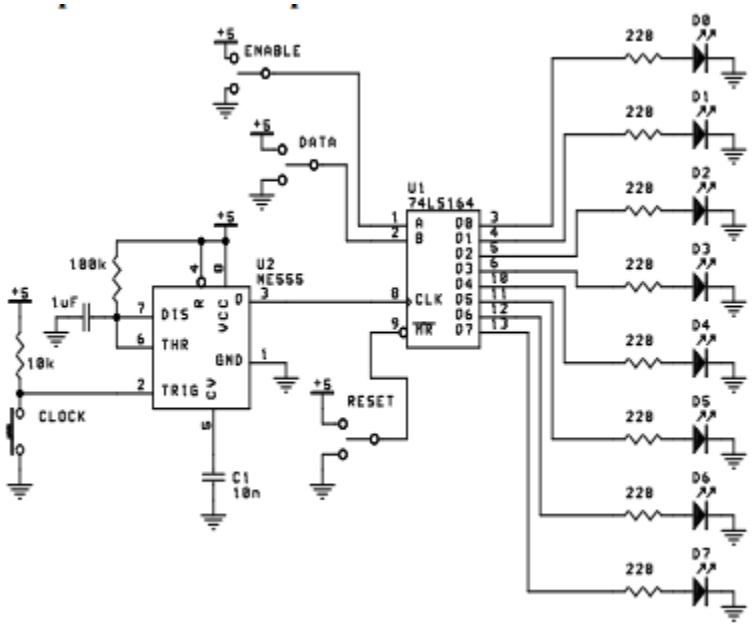


Figure.3. SIPO 74LS164

Observe Figure 5.2 above! The SIPO input consists of 1 ENABLE, 1 DATA, 1 CLK, and 1 MR (Master Reset), while the outputs consist of 8 Q0 - Q7. An additional circuit is a 555 monostable multivibrator that functions as a CLK signal generator where CLK is rising edge-triggered. All indicators use LEDs. If the LED is on, it indicates logic '1', and if it is off, it indicates logic '0'.

The steps to perform this experiment are as follows:

1. Connect the power supply by plugging the connector into the board and turn on the power supply!
2. Then fill in table 1!

3. CLK: ON means press the CLOCK push button and then release it!
4. What conclusion can you draw?

Table. SIPO Circuit Result

ENABLE	RST	DATA	CLK	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
0	X	X	X								
X	1	X	X								
1	1	0	ON								
1	1	1	ON								
1	1	0	ON								
1	1	1	ON								
1	1	0	ON								
1	1	1	ON								
1	1	0	ON								
1	1	1	ON								

b. Parallel Input Parallel Output (SIPO)

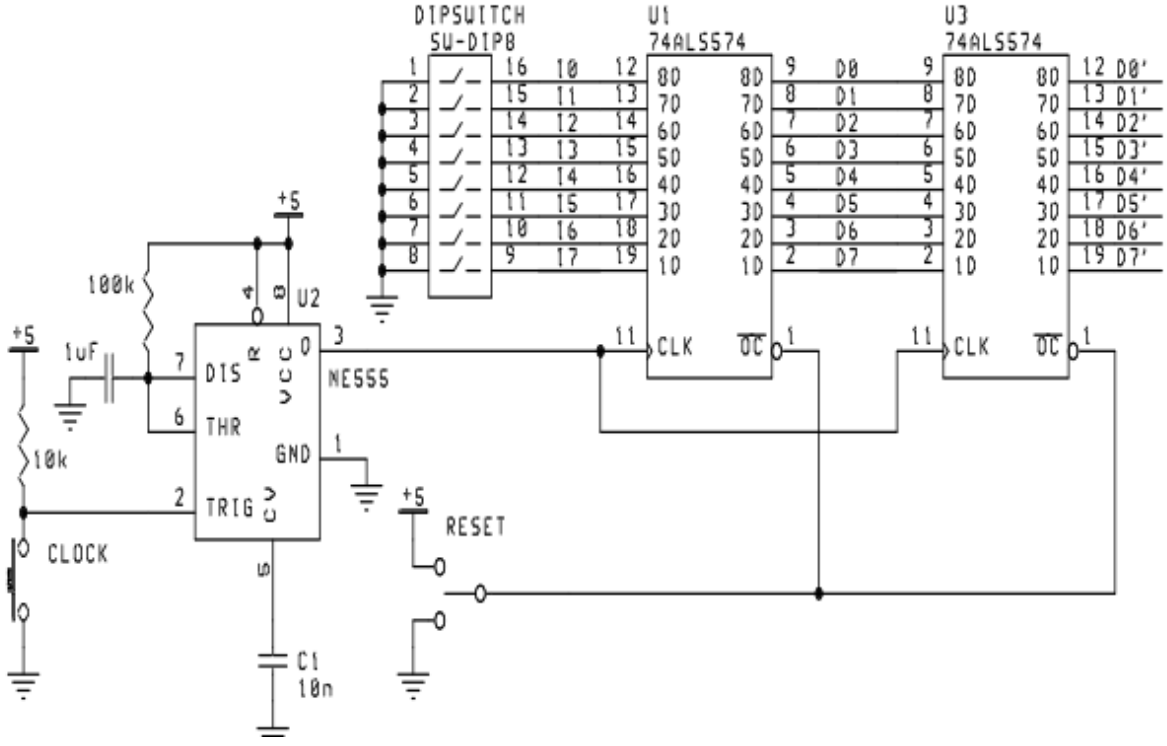


Figure.4. PIPO 74AKS574 Circuits

Observe Figure 4 above! All indicators use LEDs. If the LED is on, it indicates logic '1', and if it is off, it indicates logic '0'.

The steps to perform this experiment are as follows:

1. Connect the power supply by plugging the connector into the board and turn on the power supply!
2. Then, perform the following experiment by adjusting the dipswitches and fill in table 2!
3. CLK ON means press the CLOCK push button and then release it!
4. In row 2 of the table above, what are the conditions of D0 - D7 and D0' - D7' and so on up to row 6.

Table. 2 PIPO circuit result

Instruksi								OC	CLK	DATA 1	CLK	DATA 2
I0	I1	I2	I3	I4	I5	I6	I7					
X	X	X	X	X	X	X	X	1	X		X	
0	0	0	0	0	0	0	0	0	ON		ON	
1	1	1	1	1	1	1	1	0	ON		ON	
0	1	0	1	0	1	0	1	0	ON		ON	
1	0	1	0	1	0	1	0	0	ON		ON	
0	0	0	0	1	1	1	1	0	ON		ON	

LAB 7
DECODER

Learning Objectives

1. Able to analyze the operation of a Decoder.
2. Able to utilize a decoder for other functions.

Supporting Theory

A Decoder can be seen at a glance as a block with few inputs and many outputs. In general, a decoder has N input pins and 2N output pins. These input pins are used to provide codes for the output pins.

Logic Gates for IC 74LS138, 74LS139, and 4514

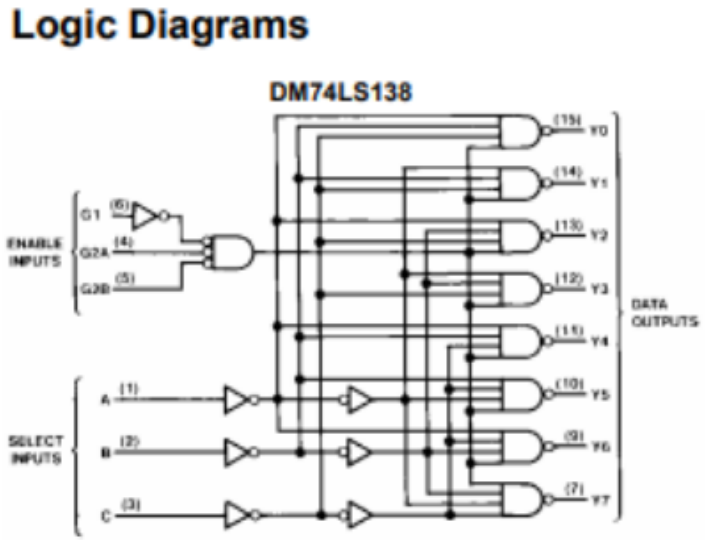


Figure.1. IC 74LS138

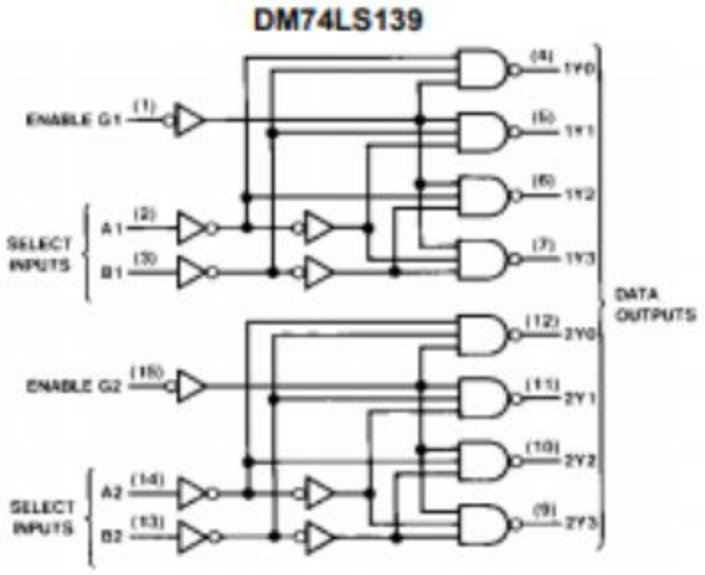


Figure.2. IC 74LS139

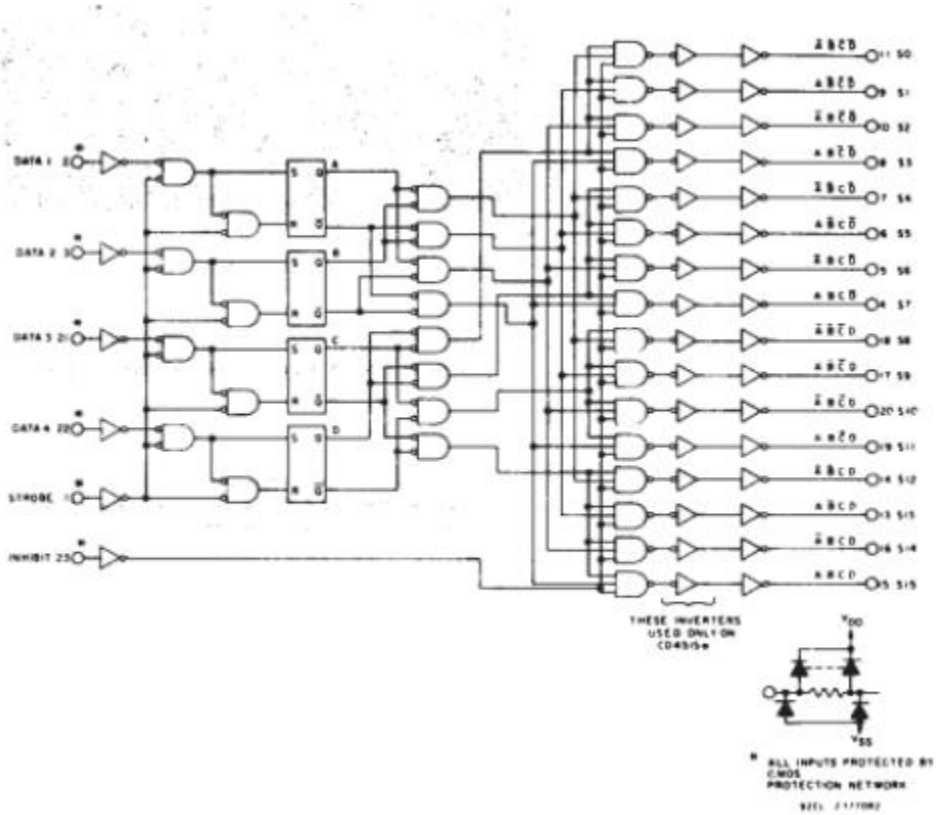


Figure.3. IC 4514

Experimental Instruction

a. Decoder 2 to 4

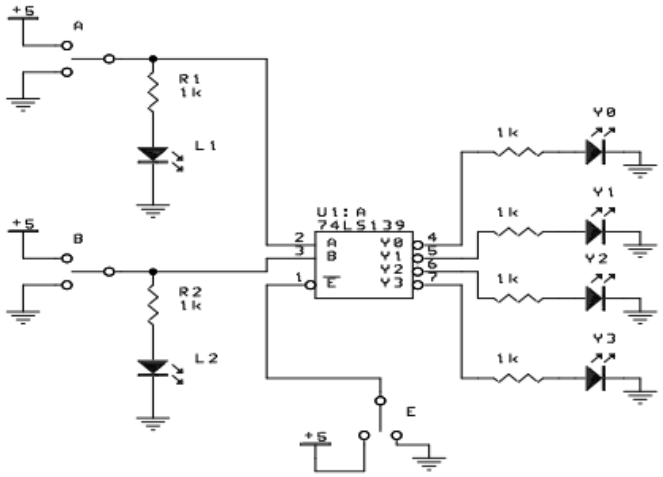


Figure.4. Circuit for decoder 2 to 4

Please observe Figure 4 above! The input to the 2-to-4 Decoder consists of 2 inputs, A and B, as well as an enable input E. All indicators for the inputs use LEDs, and the outputs also use LEDs. If the LED is on, it indicates logic '1', and if it is off, it indicates logic '0'.

The steps to perform this experiment are as follows:

1. Connect the power supply by plugging the connector into the board and turn on the power supply!
2. Then fill in table 6.1, by setting the input switches for A and B!
3. What conclusion can you draw?

Table.1. Circuit experimental of decoder 2 to 4

-E	B	A	Y3	Y2	Y1	Y0
1	X	X				
0	0	0				
0	0	1				
0	1	0				
0	1	1				

b. Decoder 3 to 8

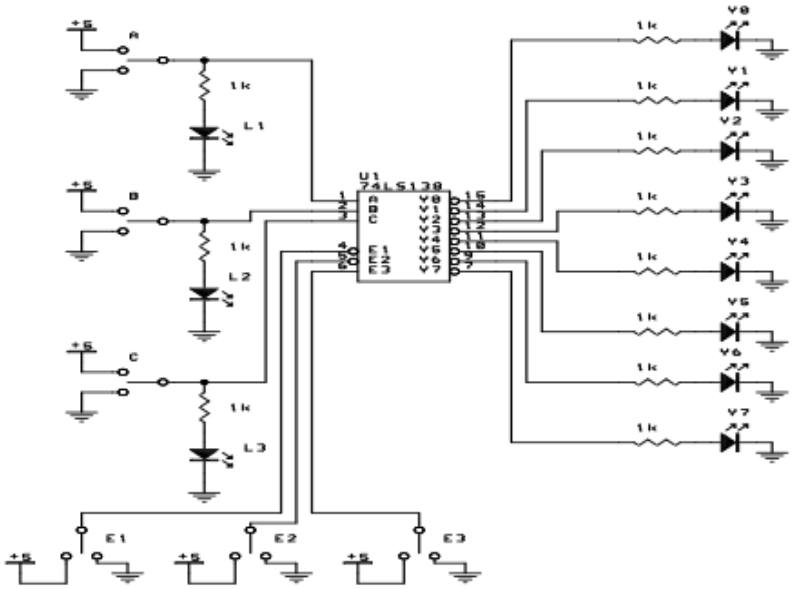


Figure.5. Circuit for decoder 3 to 8

Please observe Figure 5 above! The input to the 3-to-8 Decoder consists of 3 inputs, A, B, and C, as well as enable inputs -E1, -E2, and E3. All indicators for the inputs use LEDs, and the outputs also use LEDs. If the LED is on, it indicates logic '1', and if it is off, it indicates logic '0'.

The steps to perform this experiment are as follows:

1. Connect the power supply by plugging the connector into the board and turn on the power supply!
2. Then fill in table 2!
3. What conclusion can you draw?

Table.2. Circuit experimental of decoder 3 to 8

E1	E2	E3	C	B	A	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
1	X	X	X	X	X								
X	1	X	X	X	X								
X	X	0	X	X	X								
0	0	1	0	0	0								
0	0	1	0	0	1								
0	0	1	0	1	0								
0	0	1	0	1	1								
0	0	1	1	0	0								
0	0	1	1	0	1								
0	0	1	1	1	0								
0	0	1	1	1	1								